Amendments to the Claims:

This listing of the claims will replace all prior versions and listings of claims in the application:

Listing of the Claims:

Claims 1-9 (canceled)

10 (Previously Presented): A method of manufacturing semiconductor devices, the method comprising:

providing a semiconductor substrate comprising a SiGe layer formed on a base layer, and a silicon layer formed on the SiGe layer, wherein the semiconductor substrate comprises one or more first regions and one or more second regions spaced apart from each other by isolation regions between the first regions and the second regions;

selectively removing at least a portion of the silicon layer only in said one or more first regions;

implanting a p-type dopant in said one or more first regions and implanting an n-type dopant in said one or more second regions;

forming a gate oxide layer in said one or more first regions and said one or more second regions; and

forming a gate electrode layer over the gate oxide layer.

11 (Currently Amended): The method according to ~~claim~~ claim 21, wherein a p-type dopant is implanted in said one or more first regions and an n-type dopant is implanted in said one or more second regions.

12 (Previously Presented): The method according to claim 10, wherein substantially all of the silicon layer is removed from said one or more first regions.

13 (Previously Presented): The method according to claim 10, further comprising forming a high-k dielectric layer on the SiGe layer of said one or more first regions after removing substantially all of the silicon layer.

14 (Original): The method according to claim 13, wherein the high-k dielectric layer comprises dielectric selected from the group consisting of zirconium oxide or hafnium oxide.

15 (Original): The method according to claim 10, further comprising oxidizing the silicon layer to form the gate oxide.

16 (Previously Presented): The method according to claim 15, wherein substantially all of the remaining silicon layer in said one or more first regions is oxidized to form the gate oxide layer.

17 (Original): The method according to claim 10, wherein the silicon layer is formed to a thickness of about 50 Å to about 500 Å.

18 (Original): The method according to claim 10, wherein the gate oxide layer has a thickness of about 10 Å to about 50 Å.

19 (Original): The method according to claim 10, wherein the silicon layer comprises strained silicon.

20 (Original): The method according to claim 10, wherein the SiGe layer comprises a first sublayer and said first sublayer has a composition that is graded from about 0% Ge at the SiGe layer/base layer interface up to about 30% Ge.

21 (Previously Presented): A method of manufacturing semiconductor devices, the method comprising:

providing a semiconductor substrate comprising a SiGe layer formed on a base layer, and a silicon layer formed on the SiGe layer, wherein the semiconductor substrate comprises one or more first regions and one or more second regions spaced apart from each other by isolation regions between the first regions and the second regions;

selectively removing at least a portion of the silicon layer only in said one or more first regions;

implanting dopant in said one or more first regions and said one or more second regions; and

forming a gate oxide layer in said one or more first regions and said one or more second regions by oxidizing the silicon layer to form the gate oxide layer, wherein substantially all of the remaining silicon layer in said one or more first regions is oxidized to form the gate oxide layer.

22 (Previously Presented): The method according to claim 21, wherein the SiGe layer comprises a first sublayer and said first sublayer has a composition that is graded from about 0% Ge at the SiGe layer/base layer interface up to about 30% Ge.

23 (Previously Presented): A method of manufacturing semiconductor devices, the method comprising:

providing a semiconductor substrate comprising a SiGe layer formed on a base layer, and a silicon layer formed on the SiGe layer, wherein the semiconductor substrate comprises one or more first regions and one or more second regions spaced apart from each other by isolation regions between the first regions and the second regions;

selectively removing substantially all of the silicon layer only in said one or more first regions;

implanting dopant in said one or more first regions and said one or more second regions;

forming a gate oxide layer in said one or more first regions and said one or more second regions, wherein

said gate oxide layer is formed immediately adjacent to and in contact with the SiGe layer in said one or more first regions.

24 (Currently Amended): The method according to ~~claim~~ claim 23, wherein a p-type dopant is implanted in said one or more first regions and an n-type dopant is implanted in said one or more second regions.

25 (Previously Presented): The method according to claim 23, further comprising forming a high-k dielectric layer on the SiGe layer of said one or more first regions after removing substantially all of the silicon layer.

26 (Previously Presented): The method according to claim 25, wherein the high-k dielectric layer comprises dielectric selected from the group consisting of zirconium oxide or hafnium oxide.

27 (Previously Presented): The method according to claim 23, wherein the SiGe layer comprises a first sublayer and said first sublayer has a composition that is graded from about 0% Ge at the SiGe layer/base layer interface up to about 30% Ge.